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[Print Format](#)**Implementation of high-side, high-voltage RESUR LDMOS in a sub-half micron smart power technology**Zhu, R. Parthasarathy, V. Khemka, V. Bose, A. Roggenbauer, T.
SPS, Motorola Inc., Mesa, AZ;*This paper appears in: Power Semiconductor Devices and ICs, 2001. ISPS '01. Proceedings of the 13th International Symposium on*
06/04/2001 -06/07/2001, 2001

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On page(s): 403-406

2001

References Cited: 6

Number of Pages: xxxi+467

INSPEC Accession Number: 7092179

Abstract:

55 V high-side RESURF LDMOS has been integrated successfully in 0.35 μm smart power technology by carefully arranging the lateral doping profile. This device has $R_{\text{ds, on}}$ area of 0.55 $\text{m}\Omega\cdot\text{cm}^2$ with excellent safe operating area. With proper device terminal biasing scheme, this device can also be used as an isolated device. Techniques and issues related to the isolation is considered and discussed.

Index Terms:

doping profiles isolation technology power MOSFET power integrated circuits 0.35 μm 55 V device isolation high-side high-voltage RESURF LDMOS transistor lateral doping profile safe operating area smart power technology terminal biasing

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